1. A method of planarizing substrates having shallow trench isolation, comprising:

providing a substrate;

forming trenches in said substrate;

depositing a layer of dielectric on said substrate thereby filling said trenches with said dielectric;

forming a layer of resist on said layer of dielectric;

providing a polishing pad having a hardness of at least Shore "D" 52; and

removing said layer of resist and part of said layer of dielectric using said polishing pad and chemical mechanical polishing thereby leaving said trenches filled with trench dielectric and forming a planar surface.

2. The method of claim 1 wherein said substrate is a silicon wafer having devices formed therein.

3. The method of claim 1 wherein said dielectric is silicon dioxide deposited using high density plasma chemical vapor deposition.

4. The method of claim 1 wherein said trenches are shallow trench isolation trenches.

5. The method of claim 1 wherein said layer of resist is formed by spinning resist on said substrate followed by baking said resist.

6. The method of claim 1 wherein said resist is photoresist.

7. The method of claim 6 wherein said photoresist is formed by spinning said photoresist on said substrate followed by baking said photoresist.

8. The method of claim 1 wherein said removing said layer of resist and part of said layer of dielectric removes that part of said layer of dielectric above said top surface of said substrate.

9. The method of claim 1 further comprising:

forming a layer of pad oxide on said substrate before said forming trenches in said substrate;

forming a layer of silicon nitride on said layer of pad oxide before said forming trenches in said substrate; and

forming trench openings in said layer of pad oxide and said layer of silicon nitride before said forming trenches in said substrate.

10. The method of claim 9 wherein said removing said layer of resist and part of said layer of dielectric removes that part of said layer of dielectric above said layer of silicon nitride.

11. A method of planarizing substrates having shallow trench isolation, comprising:

providing a substrate;

forming a dielectric base on said substrate;

forming trench openings in said dielectric base;

forming trenches in said substrate directly below said trench openings in said dielectric base;

depositing a layer of trench dielectric on said dielectric base thereby filling said trenches with said trench dielectric;

forming a layer of resist on said layer of trench dielectric;

providing a polishing pad having a hardness of at least Shore "D" 52; and

removing said layer of resist and part of said layer of trench dielectric using said polishing pad and chemical mechanical polishing thereby leaving trench dielectric in said trenches and forming a planar surface.

12. The method of claim 11 wherein said substrate is a silicon substrate having devices formed therein.

13. The method of claim 11 wherein said trench dielectric is silicon dioxide deposited using high density plasma chemical vapor deposition.

14. The method of claim 11 wherein said dielectric base comprises a layer of pad oxide formed on said substrate and a layer of silicon nitride on said layer of pad oxide.

15. The method of claim 14 wherein said removing said layer of resist and part of said layer of dielectric removes that part of said layer of dielectric above said layer of silicon nitride.

16. The method of claim 11 wherein said layer of resist is formed by spinning resist on said substrate followed by baking said resist.

17. The method of claim 11 wherein said resist is photoresist.

18. The method of claim 16 wherein said photoresist is formed by spinning said photoresist on said substrate followed by baking said photoresist.

19. The method of claim 11 wherein said removing said layer of resist and part of said layer of dielectric removes that part of said layer of dielectric above said dielectric base.